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UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF OREGON
PORTLAND DIVISION

FEREYDUN TABAIAN and AHMAD ASHRAFZADEH, Plaintiffs, v. INTEL CORPORATION, Defendant.	Civil Action No.: 3:18-cv-0326-HZ **PLAINTIFFS' RESPONSE BRIEF ON CLAIM CONSTRUCTION**

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Abbreviation	Explanation
944, xx:yy (ECF 1-1)	U.S. Patent No. 7,027,944 ("the '944 Patent") (filed as ECF No. 1-1), column no. xx, line no. yy
DeRouin Decl. (Ex. A) (ECF 144-1)	U.S. Provisional Patent Application No. 60/484,105 (filed with this brief as Ex. A to DeRouin Declaration)
DeRouin Decl. (Ex. B) (ECF 144-2)	Originally Filed Claims for U.S. Patent Application No. 10/878,477 (filed with this brief as Ex. B to DeRouin Declaration)
VS Decl. (ECF 115-4)	Declaration of Vivek Subramanian, Ph.D., February 20, 2019 (filed as ECF No. 115-4)
Melvin Decl. (ECF 115-5)	Declaration of Stephen W. Melvin, Ph.D., February 21, 2019 (filed as ECF No. 115-5)
Melvin Decl. (ECF 115-6)	Declaration of Stephen W. Melvin, Ph.D., March 13, 2019 (filed as ECF No. 115-6)
JGD Decl. (Ex. C)	Hejazi Dep. Excerpts (rebuttal to Hejazi excerpts at ECF 146-2) (filed with this brief)
JGD Decl. (Ex. D)	Sadati Dep. Excerpts (rebuttal to Sadati excerpts at ECF 146-3) (filed with this brief)

II. INTRODUCTION

Plaintiffs' proposed constructions are supported by the plain meaning of the terms at issue in Claim 1, which are broad; the understanding of these broad claim terms by persons of ordinary skill in the art; the claim construction principles established by the Supreme Court and Federal Circuit; and the asserted patent's specification, including the provisional application incorporated therein and the original filed claims, showing that those broad claim terms encompass a variety of specific embodiments. Plaintiffs are not proposing, as Intel contends, "litigation-driven claim constructions."

Intel, on the other hand, has overtly focused its proposed constructions on one embodiment in Figures 1 and 2 of the patent, and at times on the accused Fully Integrated Voltage Regulator ("FIVR") technology (disregarding any embodiment).[1] Intel improperly seeks to limit the broad terms of the Claim 1 by incorporating limitations from one embodiment, or by adding limitations found nowhere in the patent, and ignores the full record of the relevant intrinsic evidence.

Intel's approach is inconsistent. Sometimes it cherry-picks limitations from an embodiment. Sometimes it seeks limitations that are contrary to the same embodiment. For example, Intel seeks a construction for "sense output(s)" that is plainly at odds with the embodiment depicted in Figures 1 and 2 of the '944 Patent and described in the related text in the specification. Intel argues that sense outputs must "adjust the circuitry that measures current," yet in Figures 1 and 2, the sense outputs clearly interface with the "adjustable sense amplifier (150)," not the "current sense circuit (140)." *Compare* ECF 145 at pp. 14-17, *with* 944, Fig. 1 (depicting current sense circuit 140, adjustable sense amplifier 150, calibration control circuit 190), 8:51-53

[1] Intel asserts that there is "undisputed evidence" that Intel does not infringe the asserted claims. *See*, *e.g.*, ECF 145 at p. 12 (discussing FIVR and a droop function). Plaintiffs dispute that.

("The adjustable sense amplifier [150] may be adjusted via the calibration control circuit 190."), *and* 944, Fig. 2 (depicting sense outputs 530), 9:31-36 ("The controller 500 adjusts the sense amplifiers of the regulator circuit via sense outputs 530…. These sense outputs 530 in one embodiment interface with the adjustable sense amplifiers via a digital to analog converter with registered input 510, and an amplifier 505."). Accordingly, claim 29 (which depends from asserted claim 1 via claim 26) expressly recites that the "calibration control circuit interfaces with said multiphase regulator by *adjusting said sense amplifiers* in each phase *via said sense outputs* . . . ." 944, Claim 29 (emphasis added). The construction of "sense outputs" must encompass the embodiment shown in Figs. 1 and 2 and claimed in dependent Claim 29. Intel's proposed construction does not. Plaintiffs' proposed construction does.

Other times, Intel seeks to limit broad claim language to the embodiment in Figure 1, as with its proposed construction for load voltage input. *See* ECF 145 at pp. 21-24 (seeking to limit load voltage input using Figure 1 of the '944 Patent). Intel looks to yet another aspect of that embodiment in its attempt to limit droop output(s). *See* ECF 145 at pp. 8-14 (arguing that droop outputs must "adjust a droop function").

Intel's approach to claim construction is wrong. Broad claim language should be construed broadly, and where reasonable to cover all relevant embodiments disclosed in the patent. Intel's attempt to limit broad claim language to one embodiment (or even a few), or in ways contrary to all embodiments, is improper. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005) (en banc) ("although the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments.").

Intel also places undue reliance on the subjective and inconclusive deposition testimony of non-party inventors. Such extrinsic evidence cannot trump the intrinsic evidence relied on by

Plaintiffs. *See Phillips*, 415 F.3d at 1317-19 ("extrinsic evidence, … including … inventor testimony, … is 'less significant than the intrinsic record in determining "the legally operative meaning of claim language."'); *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1584-85 (Fed. Cir. 1996) ("Nor may the inventor's subjective intent as to claim scope, when unexpressed in the patent documents, have any effect…. But testimony on the *technology* is far different from other expert testimony, whether it be of an attorney, a technical expert, or the inventor, on the *proper construction* of a disputed claim term, relied on by the district court in this case. The latter kind of testimony may only be relied upon if the patent documents, taken as a whole, are insufficient to enable the court to construe disputed claim terms. Such instances will rarely, if ever, occur."); *Bell Atlantic Network Services, Inc. v. Covad Communications Group, Inc.*, 262 F.3d 1258, 1268–69 (Fed. Cir. 2001) ("However, in the rare circumstance that the court is unable to determine the meaning of the asserted claims after assessing the intrinsic evidence, it may look to additional evidence that is extrinsic …. This additional extrinsic evidence includes such evidence as expert testimony, articles, and inventor testimony. … This extrinsic evidence may be used only to assist in the proper understanding of the disputed limitation; it may not be used to vary, contradict, expand, or limit the claim language from how it is defined, even by implication, in the specification or file history.").

The non-party inventors are not expert witnesses in this case. On the contrary, Mr. Hejazi repeatedly testified that he is not expert in the specific field of Intel's questions. *See* Hejazi Dep., 52:9 ("Since I am not an expert, I do not know"), 58:12-13, 80:7-14, 82:17, *and see* 49:3-6 ("none of my previous background was voltage regulators"), 128:15-25 (plaintiff Mr. Ashrafzadeh "was the expert … [i]n voltage regulators") (JGD Decl. Ex. C). Mr. Sadati also testified he was not an expert, including not an expert in understanding patent claims. Sadati Dep. 60:3 ("I am not kind

of expert"), 70:13 ("I am not expert in the kind of legal"), *and see* 126:16-17 (Intel, "Q. I am actually not asking [for] an expert opinion"), 165:25 ("Ahmad [Ashrafzadeh] was expert") (JGD Decl. Ex. D). Accordingly, their opinions on technical issues should be stricken. *See* Fed. R. of Evidence 701 ("If a witness is not testifying as an expert, testimony in the form of an opinion is limited to one that is: … (c) not based on … technical … knowledge within the scope of Rule 702."). They were not retained to study the patent, which issued over 13 years ago, and they did not do so. On the contrary, Mr. Hejazi testified that to prepare for his deposition he only "looked at the [patent] diagrams and first claim" and "very briefly" at "some of" the specification, and as "it was a long time ago" he "may have forgotten some of the details" of the patent. Hejazi Dep. 9-10 (JGD Decl. Ex. C). Mr. Sadati testified that he "glanced through the patent but I did not spend time to look at like what we did at that time long time back"; "mostly focused on the claim quickly." Sadati Dep. 13:2-4, 13:11-12 (JGD Decl. Ex. D). Accordingly, even if they were experts, their opinions should be stricken as lacking a reliable basis. *See* Fed. R. of Evid. 702. Intel quotes from a series of leading questions, to which Intel gave Plaintiffs a standing objection. Hejazi Dep. 70-71 (JGD Decl. Ex. C). Intel's leading questions were on direct examination and were not necessary to develop testimony, so they should be stricken as improper. *See* Fed. R. of Evidence 611(c) ("Leading questions should not be used on direct examination except as necessary to develop the witness's testimony.").

Intel suggests that these excerpts somehow confirm Intel's positions. *See*, *e.g.*, ECF 145 at pp. 1, 2, 10, 26, 28. They do not. The non-party inventor testimony primarily addresses one of many embodiments disclosed in the '944 Patent, without offering any expert opinion based on a *Phillips*-informed review of the patent claims, specification, and other evidence. *See, e.g.,* Hejazi Dep. 77, 78:10-11 (questioned about Figs. 1 and 2, he testifies, "Yes, that is one implementation.")

(JGD Decl. Ex. C). The testimony in no way suggests that the disputed terms should be limited to a specific embodiment. The testimony does not corroborate Intel's proposed limiting constructions. Further, to the extent the inventor's testimony contradicts the intrinsic evidence, the intrinsic evidence takes precedence. *Bell Atlantic*, 262 F.3d at 1268-69.

The Federal Circuit recently rejected Intel's approach to claim construction that imports limitations from preferred embodiments and relies on extrinsic inventor evidence. *See Cont'l Circuits LLC v. Intel Corp.*, 915 F.3d 788, 799-800 (Fed. Cir. 2019) (holding that the district court erred by accepting Intel's construction that improperly limited claim terms to a preferred embodiment). In that case, when faced with "plain language of the claims [that] does not include a repeated desmear process," and a "specification [that] does not clearly and unmistakably limit the claims to require a repeated desmear process," Intel still argued for a limiting construction that required the repeated desmear process, and sought to use extrinsic inventor documents to "confirm[] that their alleged invention was limited" to a preferred embodiment. *Id*. at 795-96. The trial court accepted Intel's arguments, but the Federal Circuit did not, stating: "absent 'clear and unmistakable' language suggesting otherwise, we conclude that the aforementioned statements do not meet the 'exacting' standard required to limit the scope of the claims to a repeated desmear process." *Id*. at 798 (citation omitted). Regarding extrinsic evidence, the Federal Circuit found that, because the intrinsic evidence did not support incorporating limitations from the preferred embodiment, the "less reliable" extrinsic evidence "does not counsel" for a construction that is inconsistent with the relevant intrinsic evidence. *Id*. at 799. Intel's attempt here to improperly limit the claims based on one or more preferred embodiments and unreliable extrinsic evidence should be rejected, as it was in *Cont'l Circuits*.

In contrast, Plaintiffs' proposed constructions accurately reflect the breadth of the claim language and are fully supported by the relevant intrinsic evidence. Accordingly, the Court should adopt Plaintiffs' proposed constructions.

III. THE PROPER SCOPE OF THE ASSERTED CLAIMS

The plain language of the asserted claims is broad, covering many embodiments discussed in the relevant intrinsic evidence, including the provisional application incorporated by reference. Neither the plain language of the asserted claims, nor the relevant intrinsic evidence, suggests limiting the disputed terms as Intel suggests.

The purpose of the invention is to help voltage regulators meet their general goals of providing constant and consistent power to a load and satisfying any unique power requirements of the load. *See* 944, 5:51-53, 7:46-49, 8:9 ("This invention may further power a circuit that requires near constant and consistent power over time," and may use calibration to help the "input load voltage meet [] load operation specifications" and satisfy any "unique power requirements"). To help achieve these goals, voltage regulators may implement a droop function, which "is used in a power supply to automatically lower the output voltage based on the output current." 944, 1:36-55. The droop function helps to properly power a load as the load current changes (i.e., load transients), while still meeting the specific voltage tolerances of the load. 944, 1:38-41. The droop function is often load specific. But the patent's discussion of that droop function is mere background of the invention, as manufacturers were already implementing it. 944, 1:41-43 ("The droop is set by the manufacturer of a processor and is based on a function of the regulator output current.").

The '944 Patent, including its provisional application, is directed to overcoming a fundamental and common problem existing in early voltage regulator circuits, including (but not

limited to) those that implement a droop function: correcting errors due to manufacturing variations, temperature changes, load requirements, or other operating conditions of a voltage regulator. *See*, *e.g.*, 944, 1:54-2:4. The '944 Patent discusses many ways to calibrate voltage regulators to reduce these errors and "to properly power a processor or IC chip according to the unique power specifications of the processor or chip." 944, Abstract (discussing "current sensing variations, static droop settings, mismatched phase outputs, and temperature variations in a multiphase power regulator."). While Intel argues that "[a]ll voltage regulators adjust voltage," Intel fails to acknowledge that early voltage regulators were bad at providing constant and consistent voltage due to the errors discussed above.

The invention disclosed by the '944 Patent provided a means for addressing some of these errors through the use of calibration data. The asserted claims broadly cover many embodiments of this invention. For example, the plain language of the asserted claims does not recite a droop function, circuitry that performs a droop function, circuitry that measures current, writing to nonvolatile memory, or an actual voltage supplied to the load. Instead, the plain language is broad enough to cover embodiments where, among other things, a droop function is ***not*** implemented or adjusted by the droop output(s), the sense outputs ***do not*** adjust circuitry that measures current, and calibration data is only ***read from*** nonvolatile memory. The asserted claims broadly claim a circuit for calibrating out some kinds of errors in a voltage regulator, improving the voltage regulator's ability to power a load under known operating conditions.

Plaintiffs respectfully request that the Court construe the disputed terms in accordance with the broad scope of the claim language and the variety of embodiments disclosed in the specification and other intrinsic evidence.

IV. PLAINTIFFS' ATTEMPTS TO COMPROMISE

Intel attempts to spin Plaintiffs' good-faith attempts to reach agreement on constructions for the disputed terms as some kind of admission. *See* ECF 145 at pp. 12, 16. Intel is wrong. A party's efforts at compromise within the Patent Local Rule 4 process are neither relevant under *Phillips*, nor admissible. *See* N.D. California PLR 2-4 (statements and disclosures under PLR 4-1 and 4-2 are not admissible for any purpose other than PLR scheduling).

V. DISPUTED TERMS AND CONSTRUCTIONS

As discussed above, Intel ignores the totality of the relevant intrinsic evidence by picking and choosing between embodiments, ignoring relevant disclosures, and even misstating the claim language. Plaintiffs' proposed constructions are driven by the totality of the intrinsic evidence and properly reflect the broad scope of the claim language.

A. "droop output(s)"

Claim Term To Be Construed	Plaintiffs' Proposed Construction	Intel's Proposed Construction
"droop output(s)"	Outputs of the calibration control circuit used to adjust voltage in circuitry, in a system that includes a droop function that can lower output voltage based on output current.	Outputs of the calibration control circuit used to adjust the droop function (i.e., the function that automatically lowers the output voltage based on the output current).

The parties do not dispute the definition of droop function. The background of the '944 Patent clearly states that a "droop function is used in a power supply to automatically lower the output voltage based on the output current." However, a plain reading of the asserted claims clearly shows that the asserted claims do not recite a droop function, nor do they recite circuitry that implements a droop function. Further, after discussing the droop function in the background, the '944 Patent never again discusses the droop function. Instead, the '944 Patent uses the word "droop" to describe a set voltage, such as providing a "droop loss." 8:64-66 ("This adjustable

droop amplifier 180 may be used to adjust the ***droop loss*** across the current sense circuit 140."). The Patent describes one embodiment in which a "droop output 550" is received by an "adjustable droop amplifier 180," which "may be used to adjust the droop loss," "may be used to drive an error circuit," "may be equivalent to adjusting the reference voltage," "may be used … to regulate the output power over variations in temperature," or may "compensate for regulator circuit variations." 944, 7:24-25, 8:64-67, 9:1-5, 19-22, 25-27, 36-40; 944, Claims 29 and 31 ("adjusting said adjustable droop amplifier via said droop output"; "where said adjustable droop amplifier is adjusted to compensate for regulator circuit variations"). The Patent described calibration data for droop outputs used to make adjustments so load voltage meets specifications. *See* 944, 5:32-39 ("By calibrating the droop and sense settings … the power supply compensates for inaccuracies in the circuit…. This calibration also provides the power supply with the necessary settings to meet the unique specifications of the load."), 5:61-63 ("droop and sense settings may be adjusted until the load voltage meets the loads specification.").

The title of the patent refers to "droop loss," not droop function: "Programmable Calibration Circuit For Power Supply Current Sensing And *Droop Loss* Compensation." 944, Title (emphasis added). Accordingly, the droop output(s) *may* adjust voltage in the regulator circuitry for a variety of reasons specified in the Patent, including to meet droop loss requirements, to meet load voltage specifications, or to compensate for regulator circuit variations; but in these embodiments, any droop function remains unchanged.

The droop function, where present, and the droop output(s) work together to provide an accurate output voltage. Plaintiffs' proposed construction properly reflects these important distinctions overlooked by Intel.

1. Plaintiffs Give Proper Weight To "Droop"

Plaintiffs' proposed construction is consistent with the intrinsic evidence: a droop output(s) is "used to adjust voltage in circuitry, in a system that includes a droop function that can lower output voltage based on output current."

Intel contends that Plaintiffs' proposed construction somehow "reads the 'droop' out of the term 'droop outputs.'" ECF 145 at p. 12. Not so. Rather, Intel's proposed construction reads the term "droop *function*" *into* claim 1, and it simply is not there.

Plaintiffs' proposed construction expressly refers to the droop function within a larger system environment, and does so while still being consistent with the claim language, which is silent regarding implementing the droop function.

The Patent acknowledges that voltage regulation systems may use circuitry that implements a "droop function." 944, 1:36. The Patent describes and claims additional circuitry for using calibration data to improve such existing voltage regulators. Accordingly, one intended use of the invention is with systems that include circuitry for implementing a droop function. That system is the environment for which the claims were written. But Claim 1, and the other asserted claims, do not recite such circuitry. Intel's accused FIVR microprocessors can infringe Claim 1, and the other asserted claims, without such circuitry, especially where, as Plaintiffs understand is the case here, Intel's accused microprocessors are designed to be used with external voltage regulators that include circuitry for implementing a droop function. *See Helferich Patent Licensing v. New York Times Co.*, 788 F.3d 1293, 1299 n. 4 (Fed. Cir. 2015) ("where a defendant's practice of a claimed invention presupposes that other persons engage in additional conduct, we have said that the additional conduct is part of 'the environment' in which the claim is practiced, and not

something the *defendant* need engage in for infringement to be found.") (emphasis in original and citations omitted).

Within this environment, the droop output(s) adjusts voltage in a regulator circuit to meet power requirements. *See* 944, 7:46-49 ("The sense outputs and the droop output then may be adjusted until the input load voltage meets load operation specifications."). That is what the invention is about. *See* 944, Abstract ("to properly power a processor or IC chip according to the unique power specifications of the processor or chip.").

In an environment where a droop function is present, a droop output(s) may adjust voltage in the regulator circuit to correct for errors that result in "droop inaccuracies." *See*, 944, 2:2-4. These droop inaccuracies are errors in voltage, which may be corrected using a droop amplifier, or by adjusting a reference voltage in the circuit. *See* 944, 9:50-52 ("adjusting the droop amplifier 180 may be equivalent to adjusting the reference voltage."). But Claim 1 does not require infringing circuitry, such as Intel's accused microprocessors, to include a "droop amplifier" or any other circuitry that implements a droop function.

2. <u>The Droop Output(s) Need Not Adjust A Droop Function</u>

Intel states that "droop outputs are outputs of the calibration control circuit used to adjust the droop function." ECF 145 at 9. The '944 Patent, however, does not state that the droop output(s) ***must*** adjust a droop function, nor does claim 1 recite circuitry for implementing a droop function.

Intel cites to its expert's declaration for the proposition that, in the Patent, the "error circuit implements [the] droop function." ECF 145 at 9.[2] Intel cites to the one embodiment of the

[2] *See also* Melvin Decl. (ECF 115-5), ¶ 15 ("In the circuit of Fig. 1, a function of automatically lowering the output voltage based on the output current is implemented by adjustable droop amplifier 180 in conjunction with error circuit 170.").

invention in Patent figure 1, and specification excerpts describing Figure 1, for the proposition that the "droop output" "may … adjust the droop amplifier [180]," which "may be used to adjust the droop loss across the current sense circuit 140" and "may be used to drive an error circuit…" ECF 145 at 9. First, as discussed, "droop loss" is not "droop function." Second, as indicated by the optional word "may," and by the Patent's description of figure 1 as merely "one embodiment" of the invention, those are optional aspects of the invention. *See* 944, 4:39 and 8:34-35 ("FIG. 1 is a schematic of one embodiment of the present invention"); *Cadence Pharmaceuticals Inc. v. Exela PharmSci Inc.*, 780 F. 3d 1364, 1369 (Fed. Cir. 2015) ("The statement in the specification that the concentration of the buffer 'may be' between 0.1 and 10 mg/ml is not limiting, because even if 'all of the embodiments discussed in the patent' included a specific limitation, it would not be 'proper to import from the patent's written description limitations that are not found in the claims themselves.'"). Claim 1 does not claim those options.

Specifically, Claim 1 does not claim an "error circuit." It does not claim a "droop amplifier." It does not claim a "current sense circuit." In short, it does not require the circuitry in Figure 1 that, according to Intel's expert, "implements [the] droop function." Claim 1 is broader than the embodiment of Figure 1.

Dependent Claims 26-36 recite the circuitry shown in Figure 1 that, according to Intel, implements the droop function, but those claims are not asserted in this case. Claim 26 depends from Claim 1 but requires additional circuitry, including an error circuit, droop amplifier, and current sense circuit:

> 26. The regulator circuit of claim 1 further comprising: … an adjustable droop amplifier, and an error circuit with an error amplifier, wherein each phase … include[s] … a current sense circuit … wherein: … said current sense circuit … feeds back … via said adjustable sense amplifier …; said adjustable sense amplifier also feeds into said adjustable droop amplifier; said droop amplifier

> drives said error circuit; and said error circuit drives each pulse width modulator on each said phase.

Intel is trying to import into independent Claim 1 those limitations of dependent Claim 26. That is improper.

Claim 26 is incorporated into dependent Claims 27-36. Accordingly, Claims 27-36 also require an "error circuit," "adjustable droop amplifier," etc. (and also add more limitations). But plaintiffs do not assert any of Claims 26-36. Thus, the "error circuit" and other circuitry that, according to Intel, "implements [the] droop function" is simply not at issue in this case. Claim 1 must not be construed to require it.

The '944 Patent, consistent with Claim 1's broad language, describes several functions that droop outputs may perform that do not implement or adjust the droop function. For example, the "adjustable droop amplifier 180 may be used to adjust the droop loss across the current sense circuit 140." 944, 8:64-66. In another embodiment, the droop outputs may be used to adjust the reference voltage directly instead of using an adjustable droop amplifier. *See id*. at 9:4-5. *See also* Melvin Decl. (ECF 115-5), ¶ 15.

Even the citations that Intel relies on for this point are completely silent regarding adjusting droop function. *See*, *e.g.*, ECF 145 at 9 (citing the 944, 5:32-35, 7:23-25, 8:64-66, which only mention a droop loss, and ***not*** a droop function). A droop loss is a lowered output voltage, ***not*** the droop function that relates the output voltage to the output current. Further, to adjust a droop function, the droop output(s) would have to implement the droop function. But even Intel recognizes that the droop output(s) do not implement a droop function. ECF 145 at 13 (stating that the "error circuit [is] used to implement the droop function") (citing Subramanian Supp. Decl. ¶ 12). The droop output(s) may only "adjust the droop loss across the current sense circuit" to

calibrate the voltage regulator, leaving the droop function unadjusted. *See*, *e.g.*, 944, 8:64-66. Intel's interpretation of the '944 Patent is flawed.

Intel also misstates what the '944 Patent discloses. For example, Intel states that "[t]he specification never states that the droop outputs merely adjust 'output voltage.'" ECF 145 at 13. This statement is flat wrong. The '944 Patent clearly states that droop output(s) may adjust an output voltage, such as by "adjusting a reference voltage." 944, 9:4-5. It clearly states that during calibration, "the droop output then may be adjusted until the input load voltage meets load operation specifications . . . ." 944, 7:47-49. Even Intel's expert recognizes that adjusting a reference voltage is a method used to adjust the output voltage in a regulator circuit. ECF 115-4 at ¶ 59 ("The control circuitry uses this signal to adjust the switches in order to modify the output voltage V_{out} so that it equals the desired reference voltage V_{ref}.").

Intel's position is indefensible.

3. Intel Relies On Inconclusive Non-Party Inventor Testimony

Intel invites the Court to draw suspect inferences from inconclusive non-party inventor testimony. For example, Intel states that one of the non-party inventors "testified unequivocally that the droop outputs are the outputs used to adjust the droop function." ECF 145 at 10. However, the testimony ***does not*** confirm that droop output(s) as recited in Claim 1 are ***only*** used to adjust a droop function. Rather, the testimony was uncertain, and merely addressed the "one embodiment" (in the Patent's words) – "one implementation" (the witnesses' words) – shown in figures 1 and 2, in which the droop output adjusts a "droop amplifier" (which in Patent figure 1, about which the witness was testifying, sends an output to an "error circuit"). *See* Hejazi Dep., 77:10 -78:

> Q. Turn to column 9, line 23 [of the Patent], and tell me when you get there?
> A. Yes.
> *****

> Q. *** It says: "The calibration control circuit 190 in FIG. 1 is shown in more detail in FIG. 2. FIG. 2 shows one embodiment of the calibration control circuit. The calibration control circuit controls the adjustments to the droop amplifier via the droop output 550 and the sense amplifiers via sense outputs 530." Did I read that correctly, sir?
> A. Yes.
> *****
> Q. The droop output of the '944 patent adjusts the droop amplifier; correct?
> A. Give me some time to look at the circuits. (Pause) Yes, that is one implementation.
> Q. And the droop amplifier adjusts the droop function; correct?
> A. I think so.

The witness was not certain that the droop amplifier adjusts the droop function, and he was testifying only about one embodiment, based on his review of figures 1 and 2 and counsel's reading of only a few lines of Patent column 9. That testimony is not relevant to Claim 1, which does not recite a "droop amplifier" (or error circuit) and is not limited to figure 1.

Again, Intel is focusing on one of many embodiments that are covered by the broad claim language. This testimony is "less reliable" extrinsic evidence that "does not counsel" for a construction limited to one embodiment. *See Cont'l Circuits*, 915 F.3d at 799 (relying on the relevant intrinsic evidence to reverse Intel's limiting construction).

B. "sense output(s)"

Claim Term To Be Construed	**Plaintiffs' Proposed Construction**	**Intel's Proposed Construction**
"sense output(s)"	Outputs of the calibration control circuit used to adjust the current feedback loop.	Outputs of the calibration control circuit used to adjust the circuitry that measures current.

A plain reading of the asserted claims, in view of the totality of the relevant intrinsic evidence, clearly shows that Intel is attempting to incorporate a limitation that would read out a preferred embodiment of the '944 Patent. This is improper. *Kaneka Corp. v. Xiamen Kingdomway Grp. Co.*, 790 F.3d 1298, 1304 (Fed. Cir. 2015) ("A claim construction that excludes a preferred

embodiment is 'rarely, if ever, correct.'") (citation omitted). In doing so, Intel attempts to blur the lines between distinct circuit components (i.e., the current sense circuit and the adjustable sense amplifier). *See* ECF 145 at 15 (stating that "the current sensing circuitry includes the current ***sense*** circuit and the ***sense*** amplifier.") (emphasis in original).

The '944 Patent is clear that sense outputs are outputs of the calibration control circuit used to adjust the current feedback loop, which may include any of the current sense circuit, adjustable sense amplifier, pulse width modulator, or another circuit component of the current sense feedback loop. *See* 944, Fig. 1, 3:29-32. Plaintiffs' proposed construction properly reflects the clear disclosure.

1. Plaintiffs Give Proper Weight To "Sense"

Intel again complains that Plaintiffs' proposed construction somehow "read the 'sense' out of 'sense outputs.'" ECF 145 at 17. Intel's attack on Plaintiffs' proposed construction ignores that Plaintiffs' proposed construction affirmatively references the current feedback loop, which measures current and feeds the measured current back to the voltage regulator. As discussed above, the current feedback loop may include any of the current ***sense*** circuit, adjustable ***sense*** amplifier, pulse width modulator, or another circuit component of the current feedback loop. *See*, *e.g.*, 944, Fig. 1, 3:29-32. Plaintiffs give proper weight to the "sense" in the asserted claims.

2. Sense Output(s) Need Not Adjust Circuitry That Measures Current

Intel appears to recognize that the adjustable sense amplifier is distinct from the current sense circuit that measures current. ECF 145 at 15 ("The ***current sense circuit measures the amount of current*** that is supplied to the load, and the ***sense amplifier amplifies (increases) the measured current signal*** so it can be used in the current feedback loop.") (emphasis added). Nevertheless, Intel still attempts to blur the lines between distinct circuit components. The '944

Patent is clear that the adjustable sense amplifier does ***not*** measure any current, which is performed by the current sense circuit:

> This ***current sense circuit may be implemented by measuring the current*** across the sense resistors, an RDS on the output FET driver, the current across the inductor of a DCR circuit, or the current across the resistance of a board trace. No matter the implementation of the current sense circuit, ***the current sense circuit feeds back to the regulator circuit through the adjustable sense amplifier*** . . .

944, 8:43-50 (emphasis added). Intel's proposed construction ignores this clear distinction. This flaw in Intel's construction is further highlighted when considering the purpose of an amplifier. By definition, an amplifier applies a gain to a signal. *Cf*. 944, 8:54-58 ("adjusting ***the feed back gain*** of the adjustable sense amplifier"). Thus, after the current is measured, the sense outputs may apply a gain to this measurement. Intel's proposed construction runs afoul of the basic purpose of the disclosed circuitry.

C. "said calibration control circuit interfaces with said nonvolatile memory to store calibration data"

Claim Term To Be Construed	Plaintiffs' Proposed Construction	Intel's Proposed Construction
"said calibration control circuit interfaces with said nonvolatile memory to store calibration data"	Plain meaning. Alternatively: The calibration control circuit communicates with nonvolatile memory to store calibration data in any memory.	The calibration control circuit writes calibration data into the nonvolatile memory.

A plain reading of asserted claim 1 reveals that the calibration control circuit need not write to nonvolatile memory. Intel ignores this clear language and attempts to improperly impose this limitation on the scope of much broader language. However, the relevant intrinsic evidence shows embodiments where the calibration control circuit interfaces with the nonvolatile memory by reading from the memory and by storing the calibration data in another type of memory. Plaintiffs' proposed construction is true to the claim language and covers both embodiments.

1. Intel Misstates The Intrinsic Evidence

Intel misstates the disputed claim language in arguing that the language somehow "requires [sic] storing calibration data in nonvolatile memory." ECF 145 at 30. Had this disputed claim language required writing to nonvolatile memory, the claim language would have stated so. Intel ignores the dependent claims that recite writing to nonvolatile memory, creating a presumption that the independent claim does ***not*** require writing to the nonvolatile memory. *Compare*, 944, Claim 1 ("to store calibration data"), *with* 944, Claim 19 ("write to nonvolatile memory"). *See Phillips*, 415 F.3d at 1315 ("[T]he presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim.").

Further, the surrounding claim language does nothing to rebut this presumption. For example, asserted claim 1 merely requires that the nonvolatile memory stores calibration data. *See* 944, Claim 1 ("said nonvolatile memory stores calibration data"). However, this language supports Plaintiffs' proposed construction, not Intel's. The calibration data stored in nonvolatile memory may be read from non-volatile memory and stored in another memory. *See*, *e.g.*, 944, 4:29-33 ("The controller then. [sic] ***references the memory for stored calibration data*** that may be associated with the sampled temperature. Finally the controller sets the sense output and the droop output of the calibration control circuit according to the calibrated data.") (emphasis added). *See also* Melvin Decl. (ECF 115-5), ¶ 25. After interfacing with nonvolatile memory, the calibration data may be stored in any type of memory.

Intel also argues that "[i]f the '944 patent's inventors had intended to cover retrieving data from nonvolatile memory and then storing it in some other type of memory, they could have written the claims to state that." ECF 145 at 33. Intel fails to appreciate that this argument cuts against Intel's own claim construction position. If asserted claim 1 required writing to nonvolatile

memory, it would have been written to include that limitation. *Compare* 944, Claim 1 ("to store calibration data") *with* 944, Claim 19 ("write to nonvolatile memory"). However, as discussed above, the disputed claim language is broad enough to cover multiple ways of interfacing with nonvolatile memory, such as reading from nonvolatile memory. Broad claim language ***can*** cover multiple embodiments as understood by a POSITA based on the disclosure. *See*, *e.g.*, *Nazomi Communications, Inc. v. ARM Holdings, PLC*, 403 F.3d 1364, 1369 (Fed. Cir. 2005) (claims may embrace "different subject matter than is illustrated in the specific embodiments in the specification").

Finally, Intel argues that giving the claim its proper breadth would not achieve the advantages achieved by the claimed invention. *See* ECF 145 at 31 (discussing "the ability to store the calibration data in nonvolatile memory so that it can still be used if the system is powered down and then re-started."). This argument is a non-starter because the surrounding claim language affirmatively recites calibration data stored in nonvolatile memory. *See* 944, Claim 1 ("said nonvolatile memory stores calibration data"). As such, Intel's proposed construction cannot be correct.

2. Intel Again Relies On Inconclusive Non-Party Inventor Testimony

Intel states that the non-party inventors "confirmed that storage of the calibration data in nonvolatile memory is an important feature of the claimed invention." ECF 145 at 32. The fact that nonvolatile memory stores calibration data is not disputed. *See* 944, Claim 1 ("said nonvolatile memory stores calibration data"). Nor it is disputed that this is an important feature of the claimed invention. However, the cited deposition testimony in no way supports limiting the disputed claim language by requiring the calibration control circuit to write to nonvolatile memory.

D. "calibration data"

Claim Term To Be Construed	Plaintiffs' Proposed Construction	Intel's Proposed Construction
"calibration data"	Data used in determining droop output and sense output settings, based in part on operating a circuit under known conditions.	Data that relates the sense outputs and droop outputs with temperature and is used to adjust those outputs as the temperature varies.

The totality of the relevant intrinsic evidence reveals that calibration data is used in determining droop output and sense output settings using known circuit conditions. For example, the asserted claims are directed to calibrating a regulator circuit to account for "power specifications [that] vary with manufacture or temperature" (944, 4:20-21), which may "vary from processor to processor, even those manufactured by the same manufacturer within the same batch" (944, 1:58-61). As such, the known conditions can include, among other things, "production variations in chip manufacture" (944, 4:11) and "temperature variation causing [] droop inaccuracies" (944, 2:3-4). Not all calibration data is used to calibrate for temperature variations. DeRouin Decl. (Ex. A), p. 4 (discussing unbalanced phase currents and providing "a calibration scheme by which the inaccuracies of the discrete [circuit] components are accounted and corrected for."). *See also* 944, Claims 6 and 7 ("nonvolatile memory stores regulator performance parameters" and/or "application specific power curve data"), 944, Claims 31 and 32 ("droop amplifier" and "sense amplifier" are "adjusted to compensate for regulator circuit variations"). Plaintiffs' proposed construction accurately reflects how broadly calibration data is used in the intrinsic evidence.

1. Intel Only Focuses On Temperature

As discussed above, in the context of the relevant intrinsic evidence, not all calibration data relates to temperature variations. Intel even argues that the words "calibration data" necessarily require incorporating a temperature limitation when construing this term. ECF 145 at 29 ("***As its***

name suggests, the calibration data is the data that is used to perform these temperature calibrations.") (emphasis added). Intel is wrong. Calibration data may be used for many reasons, including calibrating a regulator circuit for "current sensing variations, static droop settings, mismatched phase outputs, ***and*** temperature variations." 944, Abstract (emphasis added). *See also* DeRouin Decl. (Ex. A), Figs. 13 and 14, p. 5 (discussing that figures 13 and 14 of the provisional application are identical except that figure 14 adds a temperature sensor). Focusing on temperature alone ignores many of the advantages achieved by the calibration control circuit using calibration data.

2. Intel Misstates The Claim Language

In attacking Plaintiffs' proposed construction, Intel misstates the claim language. *See* ECF 145 at 28-29. Without citation, Intel states that "[t]he only calibration that occurs in the claims relates to temperature." ECF 145 at 28. However, the claim language is broad enough to cover embodiments that calibrate for temperature ***and*** for other known circuit conditions. Intel's characterization limiting the claim to calibrating for temperature variations is flawed. Nothing in the claim language forbids calibrating the regulator circuit using other known circuit conditions, such as manufacturing variations.

3. Intel Reads "Calibration" Out of "Calibration Data"

Intel claims that Plaintiffs' proposed construction reads on an output current of the regulator circuit used in implementing a droop function, and thus cannot be correct. *See* ECF 145 at 29.[3] Intel is wrong. Moreover, Intel ignores that its own construction has precisely the same

[3] Additionally, Intel again fails to acknowledge the distinction between calibrating an output voltage based on a droop setting and the droop function setting the droop.

issue: output current could relate sense and droop outputs to temperature, and output current could be used to adjust sense outputs and droop outputs.

Intel is wrong because it reads "calibration" out of the disputed language. Calibration data is used in determining droop and sense output settings based on known conditions. For example, "[t]he load voltage and the temperature may be monitored while the droop and sense settings may be adjusted until the load voltage meets the loads specification." 944, 5:54-6:9. "The data stored in the nonvolatile memory for the droop outputs and sense outputs may be based on the load voltage input and the temperature input." 944, 2:40-43. As such, nonvolatile memory stores calibration data used to calibrate the regulator circuit. Output current is not used to calibrate the regulator circuit.

E. "load voltage input"

Claim Term To Be Construed	Plaintiffs' Proposed Construction	Intel's Proposed Construction
"load voltage input"	Plain meaning. Alternatively: Input to the calibration control circuit that provides load voltage data.	Input to the calibration control circuit that provides the voltage supplied to the load.

Load voltage input does not need to be construed. If construed, the intrinsic evidence supports Plaintiffs' alternative construction. For example, the load voltage input ***may*** directly receive the actual voltage supplied to the load. *See*, *e.g.*, 944, Fig. 1 (depicting a voltage from the load 165 coupled directly to the calibration control circuit 190). Alternatively, the load voltage input ***may also*** provide load voltage data that represents the voltage supplied to the load. *See*, *e.g.*, 944, Fig. 2; 9:44-46 ("The controller samples load voltage input 570 from the regulator circuit in one embodiment via an analog to digital converter with registered output 670."). The load voltage input may provide an estimation or an approximation of the actual load voltage to the calibration control circuit, including a digital representation of the load voltage. *See* 944, Claim 13 ("said load

voltage input comprises an analog to digital converter with registered output."). As clearly shown in Fig. 2 of the '944, the load voltage input may use an analog to digital converter to provide data representing the voltage supplied to the load. Thus, the load voltage input does ***not*** have to provide the voltage supplied to the load, as suggested by Intel. However, in all cases, the load voltage input is an input to the calibration control circuit that provides load voltage data.

1. Intel Misunderstands Monitoring Load Voltage

Intel states that "the specification makes clear that the load voltage input is an input to the calibration control circuit that provides the voltage that is supplied to the load." ECF 145 at 22. In doing so, Intel relies on language stating that "the calibration control circuit may monitor the load voltage output of the current sense circuit via the load voltage input." ECF 145 at 22 (citing 944, 3:43-45, 7:25-27). "May" does not mean "must." Intel fails to appreciate that the load voltage output may be monitored by receiving load voltage data representing the voltage supplied to the load. Fig. 2 of the '944 Patent, which was cited by Intel, shows that the load voltage input may provide the calibration control circuit with a digital representation of the analog voltage supplied to the load. 944, Fig. 2; 9:44-46. The calibration control circuit may monitor the load voltage based on the digital representation. Monitoring the load voltage does not require receiving the actual analog voltage supplied to the load.

2. Plaintiffs' Proposed Construction Is Bounded

An "input to the calibration control circuit that provides load voltage data" properly defines the metes and bounds of a load voltage input. Intel claims that use of the word "data" would render Plaintiffs' proposed construction indefinite. ECF 145 at 24.[4] Intel's position is curious because

[4] Intel does not allege that load voltage input is indefinite, as evidenced by Intel's invalidity contentions.

Intel appears to understand what "data" means with respect to other disputed claim terms. *See*, *e.g.*, *supra* D (construing "calibration ***data***"); *infra* F (construing "temperature ***data*** is used . . ."). Intel appears to be arguing that a claim construction that reads on more than one embodiment is necessarily indefinite, which is wrong as a matter of law. *See Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, (2014) (holding that a patent must "inform, with reasonable certainty, those skilled in the art about the scope of the invention."). Even Intel's pre-*Nautilus* case law recognizes that "[a]bsolute clarity is not required to find a claim term definite." *See Star Sci., Inc. v. R.J. Reynolds Tobacco Co.*, 655 F.3d 1364, 1373 (Fed. Cir. 2011). Plaintiffs' proposed construction informs those skilled in the art of what is covered by a load voltage input, thus Plaintiffs' proposed construction is sufficiently definite.

F. "temperature data is used . . . to adjust said sense outputs and said droop outputs"

Claim Term To Be Construed	Plaintiffs' Proposed Construction	Intel's Proposed Construction
"temperature data is used … to adjust said sense outputs and said droop outputs"	Temperature data is a factor in the determination of one or more sense output and droop output settings.	Plain meaning, i.e., the calibration control circuit uses the temperature data to adjust both the sense outputs and the droop outputs.

The intrinsic evidence is clear that temperature data is used to set or adjust a combination of sense and droop output settings, adjusted as a pair of outputs. *See*, *e.g.*, 944, 5:61-63, 7:46-49. The intrinsic evidence is also clear that adjusting the combination of sense and droop output settings does not necessarily require changing *both* the sense settings and droop output settings when temperature changes. *See*, *e.g.*, DeRouin Decl. (Ex. A), p. 2, 5. Plaintiffs' proposed construction accurately reflects this intrinsic evidence in that temperature data is a factor in the determination of one or more sense output and droop output settings.

Despite Plaintiffs proposing a construction supported by the intrinsic evidence, Intel attempts to create a dispute by alleging that Plaintiffs are arguing that "and" really means "or" in the disputed claim language. *See* ECF 145 at 26. To the contrary, Plaintiffs submit that "and" has its ordinary broad meaning and should be understood consistently with the intrinsic evidence. *See* ECF 143 at 20. There is no controversy surrounding the meaning of "and." Further, the '944 Patent is clear that "and," along with other conjunctions, is "to be understood in the most inclusive sense possible." 944, 4:63-64. In this context, "and" denotes that the sense and droop outputs are determined as one pair of outputs.

Intel also argues that the specification does not use the exact "one or more" language in Plaintiffs' proposed construction. ECF 145 at 26. But Intel conveniently ignores that the exact "both" language it proposes is also never used in specification. The argument is pointless.

G. "said calibration control circuit interfaces with said regulator circuit via said sense outputs, said droop outputs, and said load voltage input"

Claim Term To Be Construed	Plaintiffs' Proposed Construction	Intel's Proposed Construction
"said calibration control circuit interfaces with said regulator circuit via said sense outputs, said droop outputs, and said load voltage input"	Plain meaning. Alternatively: The calibration control circuit communicates with the regulator circuit by way of the sense outputs, droop outputs, and load voltage input.	The calibration control circuit communicates with the regulator circuit by receiving the regulator's output voltage via the load voltage input and by sending adjustments to the regulator via the sense and droop outputs.

This disputed claim language does not need to be construed. This claim language merely describes communication between the calibration control circuit and the regulator circuit using the various outputs, whether that communication is direct or indirect. Intel seeks to construe this phrase by imposing limitations that are counter to the broad claim language and the intrinsic evidence. Specifically, Intel seeks to incorporate limitations from its erroneous constructions for other disputed claim terms, seeking to further limit the asserted claims. As discussed above (*supra*

E), a load voltage input ***need not*** provide the analog voltage supplied to the load to the calibration control circuit. *See*, *e.g.*, 944, Fig. 2; 9:44-46. Further, a plain reading of the disputed claim language is consistent with Plaintiff's proposed construction, not Intel's.

H. "calibration control circuit"

Claim Term To Be Construed	Plaintiffs' Proposed Construction	Intel's Proposed Construction
"calibration control circuit"	Plain meaning. Alternatively: Circuitry configured to set or adjust calibration data for use in the control of a regulator circuit.	Circuit that calibrates current sensing circuitry and a droop function over a range of temperatures.

Calibration control circuit does not need to be construed. The claim language is clear that a calibration control circuit is circuitry including a controller, sense outputs, droop outputs, load voltage input and temperature input, and an interface with non-volatile memory that stores calibration data. Intel seeks to construe this term in order to impose limitations on the asserted claims that are counter to the broad claim language and the intrinsic evidence.

Intel is correct that a "calibration control circuit" is "a circuit that calibrates." ECF 145 at 18. From there, Intel seeks to incorporate the erroneous limitations from its proposed constructions for sense outputs and droop output(s). A calibration control circuit is not required to calibrate current sensing circuitry (*see supra* B) and is not required to calibrate a droop function over a range of temperatures (*see supra* A). Intel's approach fails to align with the totality of the intrinsic evidence. Conversely, Plaintiffs' proposed construction reflects that a calibration control circuit uses calibration data to control a regulator circuit.

VI. CONCLUSION

Plaintiffs' proposed constructions are consistent with the breadth of the asserted claim language read in the context of the specification and other intrinsic evidence. For the reasons discussed above, the Court should adopt Plaintiffs' proposed constructions.

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Respectfully Submitted,

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